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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,092	12/01/2003	Akira Nagai	503.35443CC4	1404

20457 7590 05/12/2005

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EXAMINER	
DOTY, HEATHER ANNE	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,092	NAGAI ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-33* is/are pending in the application.

4a) Of the above claim(s) *17,18,30 and 31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,8-11,13,16,19-21,24-26,28 and 32* is/are rejected.

7)☒ Claim(s) *4,5,7,14,15,22,23,27,29 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/857,674.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/01/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: On page 9, line 16, change "add the like" to "and the like". On page 16, lines 17-18, "gang bonding method" is repeated. On page 23, line 18, "Have" should not be capitalized.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19, 20, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakayoshi et al. (IEEE, 1994), with Freyman et al. (U.S. 5,646,451) providing typical wire bonding temperatures, relevant to claim 20.

Regarding claim 19, Nakayoshi et al. teaches an adhesive film for packaging semiconductor devices, having an elastic modulus (Young's modulus), in a range of mounting reflow temperature for mounting the semiconductor element onto a mounting substrate, of more than 1 MPa (pg. 578, Fig. 7 and caption).

Regarding claim 20, Freyman et al. teaches that a typical wire bonding temperature is 225°C (column 1, lines 32-34), within the claimed ranges of reflow temperature and temperature for elastic modulus of the adhesive film.

The recitation "adapted to be used in ball grid array semiconductor devices, which is for adhering a semiconductor element to circuit tape" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claim 32, the recitation "wherein said circuit tape includes pads for electrical connection thereto by a ball grid array connection" further limits the preamble of claim 19, which, as presently written, does not have patentable weight.

Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Akikuni et al. (JP 6-236906).

Akikuni et al. teaches an adhesive film for semiconductor device packaging with an elastic modulus in a range of mounting reflow temperature for mounting a semiconductor element onto a mounting substrate (200-250°C) of more than 1 MPa and an elastic modulus at room temperature equal to or less than 4000 MPa (see drawing 3, 1MPa = 10^7 dyne/cm^2). The recitation "adapted to be used in ball grid array semiconductor devices, which is for adhering a semiconductor element to circuit tape" has not been given patentable weight for the reasons stated above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 8-9, 11, 13, 26, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. 5,620,928) in view of Nakayoshi et al. (IEEE, 1994) with Freyman et al. (U.S. 5,646,451) providing typical wire bonding temperatures, relevant to claims 2 and 13.

Regarding claims 1-3, Lee et al. teaches a circuit tape having a base material made of a dielectric film (column 2, lines 56-62) with an adhesive layer adapted to be used in ball grid array semiconductor devices, comprising a circuit tape whereon a circuit is formed (**84** in Fig. 4A; column 2, lines 56-62); and an adhesive layer for connecting said circuit tape to a semiconductor element (**87** in Fig. 4A; column 6, lines 11-13).

Lee et al. does not expressly teach that the adhesive layer insulates the circuit tape from the semiconductor element, that the elastic modulus of said adhesive layer, in a range of mounting reflow temperature for mounting the semiconductor element onto a mounting substrate, or in the range of 200°C - 250°C, is more than 1MPa, or that the adhesive layer is composed of an adhesive film.

Nakayoshi et al. teaches an insulating adhesive film (film D in Table 1 on page 576) used on lead on chip (LOC) structures with an elastic modulus (Young's modulus)

more than 1MPa at wire bonding temperatures (pg. 578, Fig. 7 and caption), which is typically 225°C (Freyman et al., column 1, lines 32-34). Nakayoshi et al. expressly teaches that this adhesive film offers good bondability at wire bonding temperatures (pg. 579, Conclusion), which are typically at 225°C.

Lee et al. and Nakayoshi et al. are analogous art because they are directed to a similar problem-solving area of semiconductor device packaging. Moreover, the instant specification (embodiment 5, pg. 24, line 5 – pg. 25, line 2) discloses using an LOC film as an adhesive for a circuit tape in a ball grid array semiconductor device, indicating that LOC and ball grid array arts are analogous.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the circuit tape with an adhesive layer taught by Lee et al. by using the adhesive film taught by Nakayoshi et al. to connect the circuit tape to a semiconductor element. The motivation for doing so at the time of the invention would have been because this adhesive film offers good bondability at relevant operating temperatures, as expressly taught by Nakayoshi et al.

Regarding claim 8, Lee et al. and Nakayoshi et al. together teach the circuit tape with an adhesive layer as claimed in claim 1. Nakayoshi et al. further teach that the adhesive layer has a layer of a thermoplastic resin, and the thermoplastic resin has a glass transition temperature greater than 250°C (adhesive film D, Table 1, pg. 576).

Regarding claim 9, Lee et al. and Nakayoshi et al. together teach the circuit tape with an adhesive layer as claimed in claim 1. Nakayoshi et al. further teaches that the

material of the adhesive layer has a coefficient of moisture absorption at 85°C/85%RH for 168 hours of, at most, 3% (adhesive film D, Table 1, pg. 576).

Regarding claims 11 and 13, Lee et al. teaches a circuit tape with an adhesive layer, adapted to be used in ball grid array semiconductor devices, comprising: an elongated circuit tape having a base material made of dielectric film, whereon circuits are formed (**84** in Fig. 4A); and at least one adhesive layer (**87** in Fig. 4A) each adhered continuously to said circuit tape, each adhesive layer having a size less than that of the elongated circuit tape (Fig. 4A).

Lee et al. does not expressly disclose that the adhesive layer is an adhesive film, wherein an elastic modulus of said adhesive film, in a range of mounting reflow temperature for mounting a semiconductor element onto a mounting substrate, or the range of 200 °C - 250°C, is more than 1MPa.

Nakayoshi et al. teaches an insulating adhesive film (film D in Table 1 on page 576) used on lead on chip (LOC) structures with an elastic modulus (Young's modulus) more than 1MPa at wire bonding temperatures (pg. 578, Fig. 7 and caption), which is typically 225°C (Freyman et al., column 1, lines 32-34). Nakayoshi et al. expressly teaches that this adhesive film offers good bondability at wire bonding temperatures (pg. 579, Conclusion), which are typically at 225°C.

Lee et al. and Nakayoshi et al. are analogous art because they are directed to a similar problem-solving area of semiconductor device packaging. Moreover, the instant specification (embodiment 5, pg. 24, line 5 – pg. 25, line 2) discloses using an LOC film

as an adhesive for a circuit tape in a ball grid array semiconductor device, indicating that LOC and ball grid array arts are analogous.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the circuit tape with an adhesive layer taught by Lee et al. by using the adhesive film taught by Nakayoshi et al. to connect the circuit tape to a semiconductor element. The motivation for doing so at the time of the invention would have been because this adhesive film offers good bondability at relevant operating temperatures, as expressly taught by Nakayoshi et al.

Regarding claims 26 and 28, together Lee et al. and Nakayoshi et al. teach the circuit tape with an adhesive layer as claimed in claims 1 and 11. Lee et al. further teaches that said circuit tape includes pads for electrical connection thereto by a ball grid array connection (wires **72** connected to solder balls in Fig. 4A).

Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. 5,620,928) in view of Akikuni et al. (JP 6-236906).

Regarding claim 6, Lee et al. teaches a circuit tape having a base material made of a dielectric film (column 2, lines 56-62) with an adhesive layer adapted to be used in ball grid array semiconductor devices, comprising a circuit tape whereon a circuit is formed (**84** in Fig. 4A; column 2, lines 56-62); and an adhesive layer for connecting said circuit tape to a semiconductor element (**87** in Fig. 4A; column 6, lines 11-13).

Lee et al. does not expressly teach that the adhesive layer insulates the circuit tape from the semiconductor element, that the elastic modulus of said adhesive layer, in a range of mounting reflow temperature for mounting the semiconductor element onto a

mounting substrate is more than 1MPa, or that the adhesive layer is composed of an adhesive film, or that the elastic modulus of said adhesive film at room temperature is equal to or less than 4000 MPa.

Akikuni et al. teaches an adhesive film for semiconductor device packaging with an elastic modulus in a range of mounting reflow temperature for mounting a semiconductor element onto a mounting substrate (200-250°C) of more than 1 MPa and an elastic modulus at room temperature equal to or less than 4000 MPa (see drawing 3, 1MPa = 10^7 dyne/cm^2).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the circuit tape with an adhesive layer taught by Lee et al. by using the adhesive film taught by Akikuni et al. to connect the circuit tape to a semiconductor element. The motivation for doing so at the time of the invention would have been because this adhesive film does not corrode at high temperatures, as taught by Akikuni et al. (abstract).

Regarding claim 16, Lee et al. teaches a circuit tape with an adhesive layer, adapted to be used in ball grid array semiconductor devices, comprising: an elongated circuit tape having a base material made of dielectric film, whereon circuits are formed (**84** in Fig. 4A); and at least one adhesive layer (**87** in Fig. 4A) each adhered continuously to said circuit tape, each adhesive layer having a size less than that of the elongated circuit tape (Fig. 4A).

Lee et al. does not expressly disclose that the adhesive layer is an adhesive film, wherein an elastic modulus of said adhesive film, in a range of mounting reflow

temperature for mounting a semiconductor element onto a mounting substrate is more than 1MPa, or that the adhesive layer is composed of an adhesive film, or that the elastic modulus of said adhesive film at room temperature is equal to or less than 4000 MPa.

Akikuni et al. teaches an adhesive film for semiconductor device packaging with an elastic modulus in a range of mounting reflow temperature for mounting a semiconductor element onto a mounting substrate (200-250°C) of more than 1 MPa and an elastic modulus at room temperature equal to or less than 4000 MPa (see drawing 3, 1MPa = 10^7 dyne/cm^2).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the circuit tape with an adhesive layer taught by Lee et al. by using the adhesive film taught by Akikuni et al. to connect the circuit tape to a semiconductor element. The motivation for doing so at the time of the invention would have been because this adhesive film does not corrode at high temperatures, as taught by Akikuni et al. (abstract).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-3 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,114,753. Although the conflicting claims are not identical, they are not patentably distinct from each other because one of ordinary skill in the art of semiconductor packaging would know that the temperature range 200°-250°C recited in claim 1 of U.S. Patent No. 6,114,753 is a specific example of a range of mounting reflow temperatures for mounting a semiconductor element onto a mounting substrate, recited in claim 1 of the instant application. Furthermore, the circuit tape claimed in claim 1 of U.S. Patent No. 6,114,753 must inherently be dielectric or the circuit elements on the circuit layer would be electrically shorted to each other. All other limitations of claims 1-3 of the instant application are recited in claim 1 of U.S. Patent No. 6,114,753. Therefore, the invention defined in claims 1-3 of the instant application is an obvious variation of the invention defined in claim 1 of U.S. Patent No. 6,114,753.

The recitation "adapted to be used in ball grid array semiconductor devices" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Claim 6 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 4 of U.S. Patent No. 6,114,753. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the reasons stated above for rejecting claim 3 of the instant application over claim 1 of U.S. Patent No. 6,114,753. The subject matter of claim 6 that further limits claim 3 of the instant application is identical to the subject matter of claim 4 that further limits claim 1 of U.S. Patent No. 6,114,753.

Claim 8 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 7 of U.S. Patent No. 6,114,753. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the reasons stated above for rejecting claim 1 of the instant application over claim 1 of U.S. Patent No. 6,114,753. The subject matter of claim 8 that further limits claim 1 of the instant application is identical to the subject matter of claim 7 that further limits claim 1 of U.S. Patent No. 6,114,753.

Claim 9 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 8 of U.S. Patent No. 6,114,753. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the reasons stated above for rejecting claim 1 of the instant application over claim 1 of U.S. Patent No. 6,114,753. The subject matter of claim 9 that further limits claim 1 of the instant application is identical to the subject matter of claim 8 that further limits claim 1 of U.S. Patent No. 6,114,753.

Claim 10 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 10 of U.S. Patent No. 6,114,753. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the reasons stated above for rejecting claim 1 of the instant application over claim 1 of U.S. Patent No. 6,114,753. The subject matter of claim 10 that further limits claim 1 of the instant application is identical to the subject matter of claim 10 that further limits claim 1 of U.S. Patent No. 6,114,753.

Claims 24 and 25 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 9 of U.S. Patent No. 6,114,753. Although the conflicting claims are not identical, they are not patentably distinct from each other because one of ordinary skill in the art of semiconductor packaging would know that the temperature range 200°-250°C recited in claim 1 (included in claim 9) of U.S. Patent No. 6,114,753 is a specific example of a range of mounting reflow temperatures for mounting a semiconductor element onto a mounting substrate, recited in claim 24 of the instant application. Furthermore, the circuit tape

claimed in claim 1 (included in claim 9) of U.S. Patent No. 6,114,753 must inherently be dielectric or the circuit elements on the circuit layer would be electrically shorted to each other. All other limitations of claim 24 of the instant application are recited in claim 9 of U.S. Patent No. 6,114,753. Therefore, the invention defined in claim 24 of the instant application is an obvious variation of the invention defined in claim 9 of U.S. Patent No. 6,114,753.

Allowable Subject Matter

Claims 4, 5, 7, 14-15, 22-23, 27, 29, and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach or suggest a three-layer adhesive structure with a porous support layer and two adhesive layers respectively applied onto both sides of said porous support layer, or a structure wherein an adhesive agent is impregnated into a porous support, with an elastic modulus greater than 1MPa in a range of mounting reflow temperatures. Prior art also does not teach or suggest an adhesive layer with a room-temperature elastic modulus lower than the elastic modulus in a temperature range of 200°-250°C, wherein the elastic modulus in a range of mounting reflow temperature is greater than 1 MPa. Finally, prior art does not teach or suggest an adhesive layer having both an elastic modulus of at most 2000 MPa in a range of –55°C to 150°C and an elastic modulus in a range of mounting reflow temperature is greater than 1 MPa.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

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PRIMARY EXAMINER